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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/340,074	06/25/99	ARIMILLI R	AT9-98-781

EXAMINER	
TZENG, F	
ART UNIT	**PAPER NUMBER**
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DATE MAILED: 12/19/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/340,074	Arimilli et al
Examiner	**Group Art Unit**
Fred Tzeng	2186

☒ Responsive to communication(s) filed on *Jun 25, 1999* .

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-21* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-21* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Drawings

1. The drawings are objected to as indicated on the attached form PTO 948. Correction is required.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

3. The blank lines on page 1 need to be filled with appropriate information.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Patel et al (USPN 5,737,751).

As to claim 1, Patel discloses a method of operating a multi-level cache of a computer system (see column 2 lines 20-24), comprising the steps of: monitoring cache activity of an upper level cache and a lower level cache both associated with a processor of the computer system (i.e., monitoring the cache activity of L1 cache 14 and L2 cache 20 which are both associated with the processor 12 of the computer system 10; see figure 2 and column 5 lines 42-63); issuing a request from the processor to load a value, wherein the request misses the upper level cache and the lower level cache (i.e., the processor 12 issues memory request to the multi-level storage system which comprises L1 cache 14 and L2 cache 20, wherein the request misses both the L1 cache 14 and L2 cache 20; see column 5 lines 42-44, 59-63); and selecting a victim cache block in the lower level cache for receiving the requested value based at least in part on the prior cache activity of the upper level cache (i.e., the reload queue of the L2 cache is selected for receiving the requested value for sending to both L1 cache and L2 cache based on the prior cache misses activity of L1 cache; see column 3 lines 5-10). By this rationale, claim 1 is rejected.

As to claim 2, Patel discloses that the victim cache block is further selected based in part on the cache activity of the lower level cache (i.e., the reload queue of L2 cache is selected not only based on the cache miss activity of L1 cache, but also based on the cache miss activity of the lower level L2 cache; see column 3 lines 5-10). By this rationale, claim 2 is rejected.

As to claim 3, Patel discloses that the selecting step takes place out of a critical path of execution of a core of the processor (i.e., the selecting steps are taking place from the execution unit of processor 12; see column 4 lines 40-50). By this rationale, claim 3 is rejected.

As to claim 4, Patel discloses that the issuing step issues a request to load operand data (i.e., the CPU requests a block of data or instructions from cache; see column 1 lines 66-67). By this rationale, claim 4 is rejected.

As to claim 5, Patel discloses that the selecting step includes the step of identifying a less recently used cache block in the lower level cache (see column 3 lines 27-30).

As to claim 6, Patel discloses the steps of: returning the requested value to the processor, determining that it would be efficient to currently load into the upper level cache a cache line which includes the requested value and in response to the determining step, loading the cache line into the upper level cache (i.e., when the processor issues a store request for data, the requested data is loaded only to the upper level L1 cache and the processor; see column 4 lines 4-7). By this rationale, claim 6 is rejected.

As to claims 7 and 9, Patel discloses that the monitoring step monitors cache misses of the upper level and lower level cache and the selecting step selects the victim cache block based at least in part on the cache misses of the lower level cache (see column 5 lines 59-63). By this rationale, claims 7 and 9 are rejected.

As to claim 8, Patel discloses the monitoring step monitors cache hits of the upper level cache and the selecting step selects the victim cache block based at least in part on the cache hits of the upper level cache (see figure 3). By this rationale, claim 8 is rejected.

As to claim 10, Patel discloses the steps of selecting a victim cache block in the upper level cache for receiving the requested value based at least in part on the cache activity of the

lower level cache (i.e., when the processor issues a store request after detecting the memory request misses of both L1 cache and L2 cache, the retrieved cache lines are stored in the upper level L1 cache only; see column 4 lines 4-7). By this rationale, claim 10 is rejected.

As to claim 11, Patel discloses a computer system (i.e., the computer system 10 depicted in figure 2; see column 4 lines 37-38), comprising: a system memory device (i.e., the main memory 22 in figure 2; see column 5 lines 8-11); means for processing program instructions (i.e., the processor 12; see column 4 lines 40-50); means connected to the processing means for caching values stored in the system memory device, the caching means having at least an upper level cache and a lower level cache both associated with the processing means (i.e., the upper level L1 cache 14 and lower level L2 cache; see figure 2 and column 4 lines 51-67); means for monitoring cache activity of the upper level cache and lower level cache (see column 5 lines 59-63); and means for selecting a victim cache block in the lower level cache for receiving a value specified in a load request issued by the processing means, wherein the load request missed the upper level cache and the lower level cache, based at least in part on the cache activity of the upper level cache (see column 3 lines 5-10). By this rationale, claim 11 is rejected.

As to claim 12, Patel discloses that the selecting means is located out of a critical path of execution of a core of the processing means (i.e., the execution unit of processor 12; see column 4 lines 40-50). By this rationale, claim 12 is rejected.

As to claim 13, Patel discloses that the upper level cache is an operand data cache (i.e., the L1 Icache and L1 Dcache; see column 2 lines 34-35). By this rationale, claim 13 is rejected.

As to claim 14, Patel discloses that the selecting means identifies a less recently used cache block in the upper level cache (see column 3 lines 27-34). By this rationale, claim 14 is rejected.

As to claim 15, Patel discloses that the upper level cache is an L1 cache and the lower level cache is an L2 cache (see figure 2 and column 4 lines 51-67). By this rationale, claim 15 is rejected.

As to claim 16, Patel discloses that the upper level cache is a store-through cache (i.e., any data stored in the upper level L1 cache is also stored in the L2 cache; see column 2 lines 36-45). By this rationale, claim 16 is also rejected.

As to claim 17, Patel discloses the means for returning the requested value to the processing means in response to the load request missing the upper level cache and the means for loading a cache line which includes the requested value into the upper level cache in response to a determination that it would be efficient to currently load the cache line into the upper level cache (i.e., when the processor issues a store request for data, the requested data is loaded only to the upper level L1 cache and the processor; see column 4 lines 4-7). By this rationale, claim 17 is rejected.

As to claim 18, Patel discloses that the monitoring means monitors cache misses of the lower level cache and the selecting means selects the victim cache block based at least in part on the cache misses of the lower level cache (see column 5 lines 59-63). By this rationale, claim 18 is rejected.

As to claim 19, Patel discloses that the monitoring means monitors cache hits of the upper level cache and the selecting means selects the victim cache block based at least in part on the cache hits of the upper level cache (see figure 3). By this rationale, claim 19 is rejected.

As to claim 20, Patel discloses that the monitoring means also monitors cache misses of the upper level and lower level caches and the selecting means selects the victim cache block based in part on the cache misses of the lower level cache (see column 5 lines 59-63). By this rationale, claim 20 is rejected.

As to claim 21, Patel discloses the means for selecting a victim cache block in the upper level cache for receiving the requested value based at least in part on the cache activity of the lower level cache (i.e., when the processor issues a store request after detecting the memory request misses of both L1 cache and L2 cache, the retrieved cache lines are stored in the upper level L1 cache only; see column 4 lines 4-7). By this rationale, claim 21 is rejected.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. **Any response to this office action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051, (formal communications, please mark "EXPEDITED PROCEDURE")

Or:

(703) 308-6606 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2021 Crystal Drive, Arlington. V.A., Sixth Floor (receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred F. Tzeng whose telephone number is (703) 305-4841. The examiner can normally be reached on weekdays from 9:30 am to 6:00 pm. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-9731.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Fred F. Tzeng

December 16, 2000

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
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